Plug & Play Memory series

2Kbit Serial I2C BUS EEPROM For SPD DRAM Memory Module

Pb Free
ROHM Electronic Components

BR34L02-W

●DESCRIPTION

BR34L02-W is 2Kbit Serial I2C BUS Electrically Erasable PROM (based on Serial Presence Detect) for DRAM Memory Module

●FEATURES

- 256×8 bit architecture serial EEPROM
- Wide operating voltage range (1.7V～5.5V)
- Two wire serial interface
- High reliability connection of Au pad and Au wire
- Self-Timed Erase and Write Cycle
- Page Write Function(16byte)
- Write Protect Mode
  - Write Protect 1(Onetime Rom) : 00h～7Fh
  - Write Protect 2(Hardwire WP PIN) : 00h～FFh
- Low Power consumption
  - Write (5V) : 1.2mA (Typ.)
  - Read (5V) : 0.2mA(Typ.)
  - Standby (5V) : 0.1μA(Typ.)
- DATA security
  - Write protect feature (WP pin)
  - Inhibit to WRITE at low V_{CC}
- Small package ------ SSOP-B8/TSSOP-B8
- High reliability fine pattern CMOS technology
- Endurance : 1,000,000 erase / write cycles
- Data retention : 40 years
- Filtered inputs in SCL / SDA for noise suppression
- Initial data FFh in all address

●BR34L02-W Series

Capacity	Bit format	Type	Power source voltage	SSOP-B8	TSSOP-B8
2Kbit	256×8	BR34L02-W	1.7～5.5V	●	●

●ABSOLUTE MAXIMUM RATING (Ta=25℃)

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	-0.3～+6.5	V
Power Dissipation	Pd	300(SSOP-B8) *1	mW
		330(TSSOP-B8) *2	
Storage Temperature	Tstg	-65～+125	℃
Operating Temperature	Topr	-40～+85	℃
Terminal Voltage	-	-0.3～Vcc+0.3	V

※ Degradation is done at 3.0mW/℃(*1), 3.3mW/℃(*2) for operation above 25℃

●RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	1.7～5.5	V
Input Voltage	V IN	0～Vcc	V

●MEMORY CELL CHARACTERISTICS (Ta=25℃, Vcc=1.7～5.5V)

Parameter	Specification			Unit
	Min.	Typ.	Max.	
Write / Erase Cycle *1	1,000,000	—	—	Cycles
Data Retention *1	40	—	—	Years

*1:Not 100% TESTED

●DC OPERATING CHARACTERISTICS (Unless otherwise specified Ta=-40～85℃, Vcc=1.7～5.5V)

Parameter	Symbol	Specification			Unit	Test Condition
		Min.	Typ.	Max.		
"H" Input Voltage 1	VIH1	0.7 Vcc	—	—	V	2.5V≦Vcc≦5.5V
"L" Input Voltage 1	VIL1	—	—	0.3 Vcc	V	2.5V≦Vcc≦5.5V
"H" Input Voltage 2	VIH2	0.8 Vcc	—	—	V	1.7V≦Vcc＜2.5V
"L" Input Voltage 2	VIL2	—	—	0.2 Vcc	V	1.7V≦Vcc＜2.5V
"L" Output Voltage 1	VOL1	—	—	0.4	V	IOL=3.0mA, 2.5V≦Vcc≦5.5V(SDA)
"L" Output Voltage 2	VOL2	—	—	0.2	V	IOL=0.7mA, 1.7V≦Vcc＜2.5V(SDA)
Input Leakage Current 1	ILI1	-1	—	1	μA	VIN=0V～Vcc(A0,A1,A2,SCL)
Input Leakage Current 2	ILI2	-1	—	15	μA	VIN=0V～Vcc(WP)
Output Leakage Current	ILO	-1	—	1	μA	VOUT=0V～Vcc (SDA)
Operating Current	ICC1	—	—	2.0	mA	Vcc =5.5V,fSCL=400kHz, tWR=5ms Byte Write Page Write Write Protect
	ICC2	—	—	0.5	mA	Vcc =5.5V,fSCL=400kHz Random Read Current Read Sequential Read
Standby Current	ISB	—	—	2.0	μA	Vcc =5.5V,SDA,SCL= Vcc A0,A1,A2=GND,WP=GND

○ This product is not designed for protection against radioactive rays.

●AC OPERATING CHARACTERISTICS（Unless otherwise specified Ta=-40～85℃, Vcc =1.7～5.5V）

Parameter	Symbol	FAST-MODE 2.5V≦Vcc≦5.5V			STANDARD-MODE 1.7V≦Vcc≦5.5V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock Frequency	fSCL	–	–	400	–	–	100	kHz
Data Clock High Period	tHIGH	0.6	–	–	4.0	–	–	μs
Data Clock Low Period	tLOW	1.2	–	–	4.7	–	–	μs
SDA and SCL Rise Time *1	tR	–	–	0.3	–	–	1.0	μs
SDA and SCL Fall Time *1	tF	–	–	0.3	–	–	0.3	μs
Start Condition Hold Time	tHD:STA	0.6	–	–	4.0	–	–	μs
Start Condition Setup Time	tSU:STA	0.6	–	–	4.7	–	–	μs
Input Data Hold Time	tHD:DAT	0	–	–	0	–	–	ns
Input Data Setup Time	tSU:DAT	50	–	–	50	–	–	ns
Output Data Delay Time	tPD	0.1	–	0.9	0.2	–	3.5	μs
Output Data Hold Time	tDH	0.1	–	–	0.2	–	–	μs
Stop Condition Setup Time	tSU:STO	0.6	–	–	4.7	–	–	μs
Bus Free Time	tBUF	1.2	–	–	4.7	–	–	μs
Write Cycle Time	tWR	–	–	5	–	–	5	ms
Noise Spike Width (SDA and SCL)	tI	–	–	0.1	–	–	0.1	μs
WP Hold Time	tHD：WP	0	–	–	0	–	–	ns
WP Setup Time	tSU：WP	0.1	–	–	0.1	–	–	μs
WP High Period	tHIGH：WP	1.0	–	–	1.0	–	–	μs

*1：Not 100％ TESTED

■ABOUT FAST-MODE AND STANDARD-MODE

Fast-mode and Standard-mode is the same operation. So it doesn't mean the different operation. It is only distinguished by frequency of operation. It defines that the operation up to 100kHz is named "Standard-mode" and the one up to 400kHz is "Fast-mode".

The value of clock frequency is maximum, it is possible to use the device up to 100kHz in Fast-mode. Lower the power supply is, more difficult it is to operate in high speed. Under Vcc=2.5V-5.5V, it is operated with 400kHz, Fast-mode (the same as Standard-mode). Under Vcc=1.7V-2.5V, it is only operate with up to 100kHz.

●SYNCHRONOUS DATA TIMING

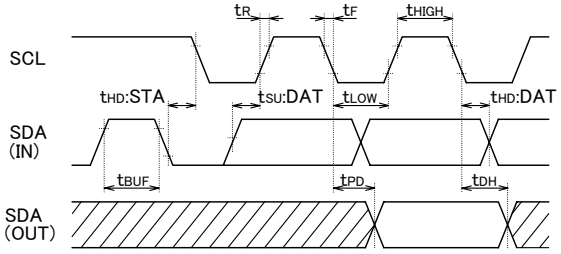


Fig.1-(a) SYNCHRONOUS DATA TIMING

○ SDA data is latched into the chip at the rising edge of SCL clock.

○ Output data toggles at the falling edge of SCL clock.

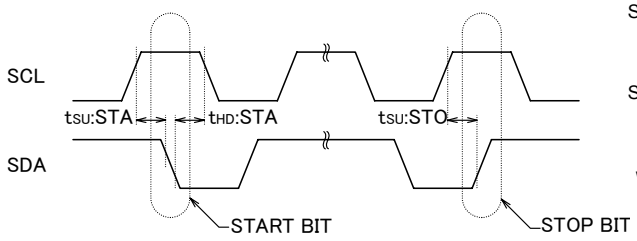


Fig.1-(b) START/STOP BIT TIMING

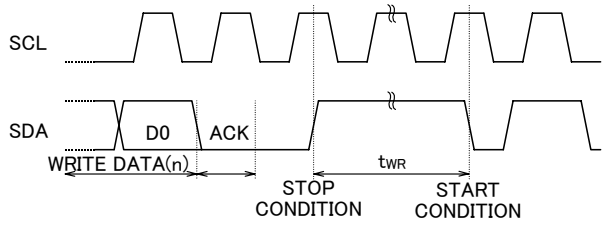


Fig.1-(c) WRITE CYCLE TIMING

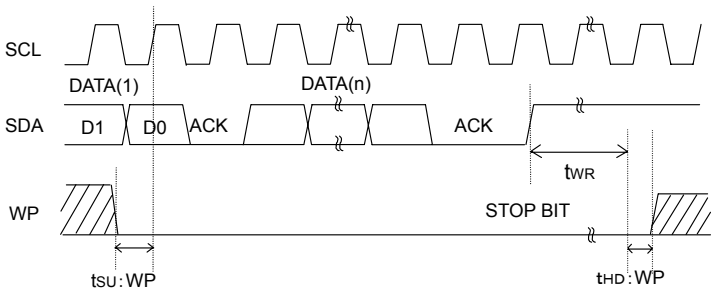


Fig.1-(d) WP TIMING OF THE WRITE OPERATION

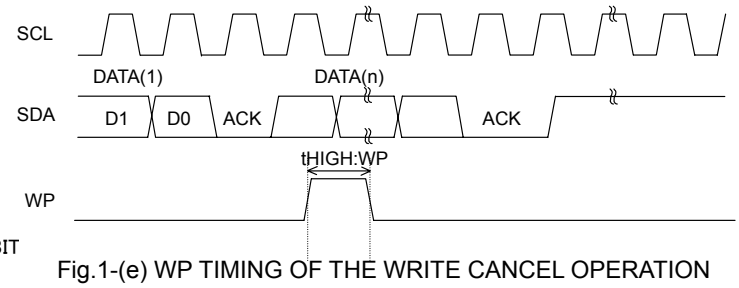


Fig.1-(e) WP TIMING OF THE WRITE CANCEL OPERATION

○For the WRITE operation, WP must be "LOW" during the period of time from the rising edge of the clock which takes in D0 of first byte until the end of tWR. (See Fig.-1 (d)) During this period, WRITE operation is canceled by setting WP "HIGH". （See Fig.-1 (e)）

○In the case of setting WP "HIGH" during tWR, WRITE operation is stopped in the middle and the data of accessing address is not guaranteed. Please write correct data again in the case.

●BLOCK DIAGRAM

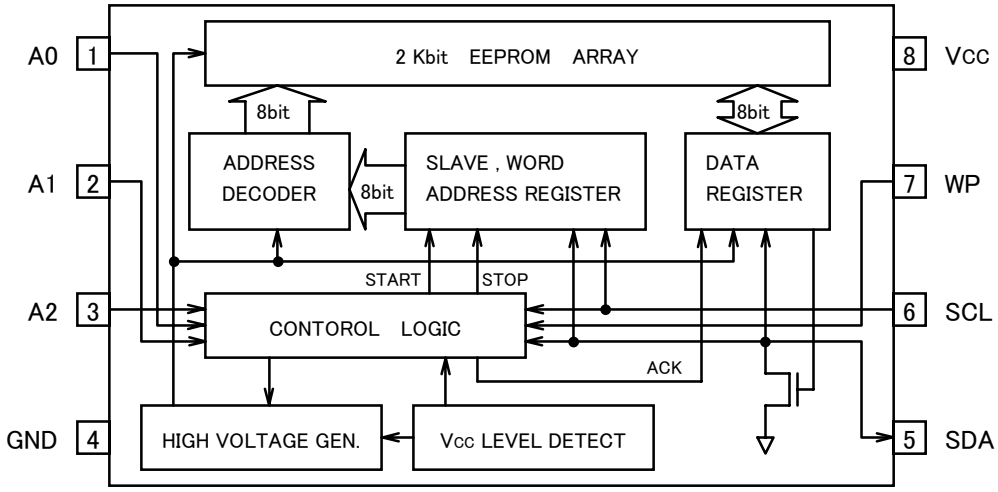


Fig.2 BLOCK DIAGRAM

●PIN CONFIGURATION AND EXPLANATION

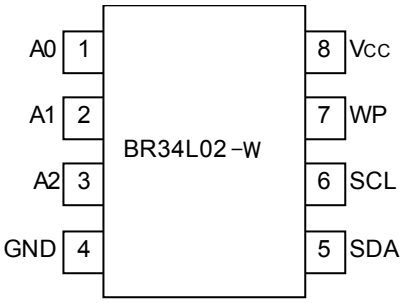


Fig.3 PIN CONFIGURATION

PIN NAME	INPUT/OUTPUT	FUNCTIONS
Vcc	–	Power Supply
GND	–	Ground 0V
A0,A1,A2	IN	Slave Address Set.
SCL	IN	Serial Clock Input
SDA	IN / OUT	Slave and Word Address, Serial Data Input, Serial Data Output *1
WP	IN	Write Protect Input *2

*1 An open drain output requires a pull-up resistor.

*2 WP Pin has a Pull-Down resistor. Please be left unconnected or connect to GND when WP feature is not in use.

●CHARACTERISTICS DATA

The following characteristic data are typ value.

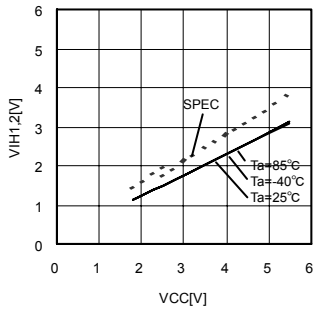


Fig.4 "H" Input Voltage VIH1,2 (A0,A1,A2,SCL,SDA,WP)

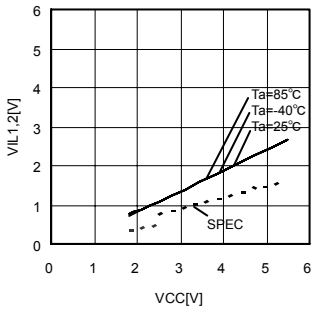


Fig.5 "L" Input Voltage VIL1,2 (A0,A1,A2,SCL,SDA,WP)

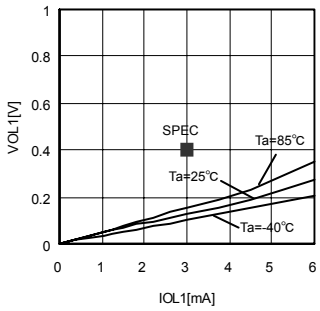


Fig.6 "L" Output Voltage VOL1-IOL1 (Vcc=2.5V)

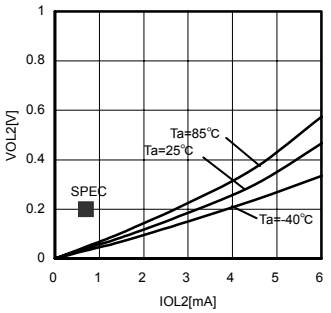


Fig.7 "L" Output Voltage VOL2-IOL2 (Vcc=1.7V)

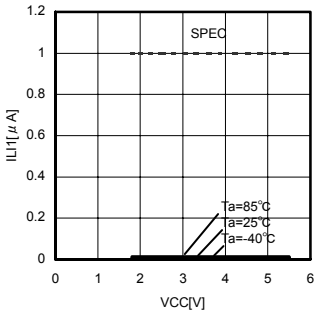


Fig.8 Input Leakage Current ILI1 (A0,A1,A2,SCL,SDA)

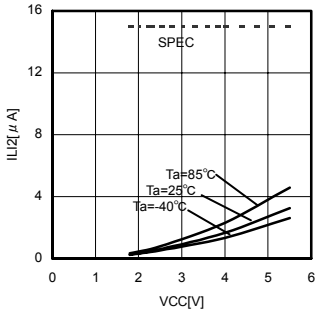


Fig.9 Input Leakage Current ILI2 (WP)

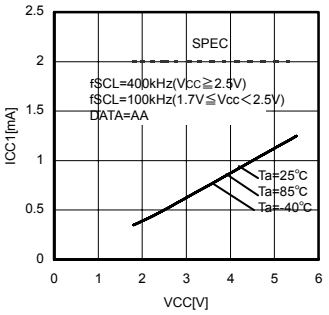


Fig.10 Write Operating Current
ICC1 (fSCL=100kHz,400kHz)

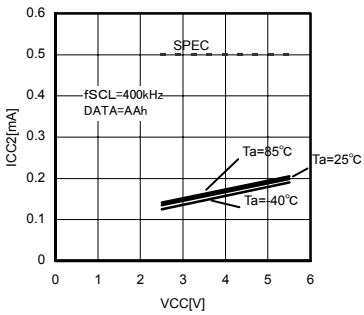


Fig.11 Read Operating Current
ICC2 (fSCL=400kHz)

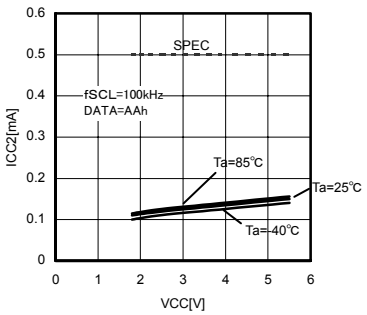


Fig.12 Read Operating Current
ICC2 (fSCL=100kHz)

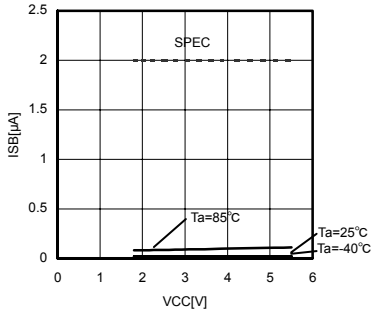


Fig.13 Standby Current
ISB

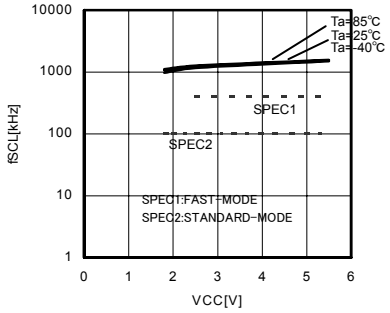


Fig.14 Clock Frequency
fSCL

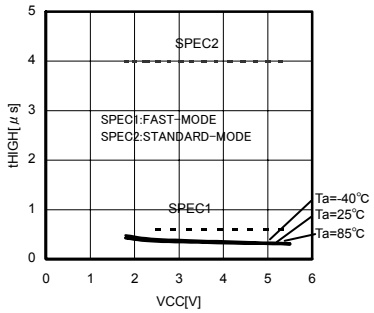


Fig.15 Data Clock High Period
tHIGH

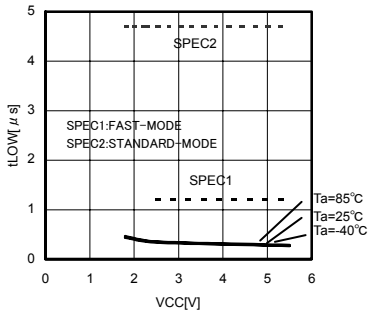


Fig.16 Data Clock Low Period
tLOW

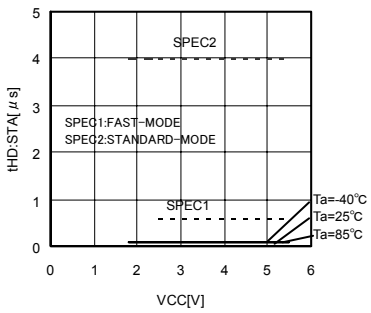


Fig.17 Start Condition Hold Time
tHD:STA

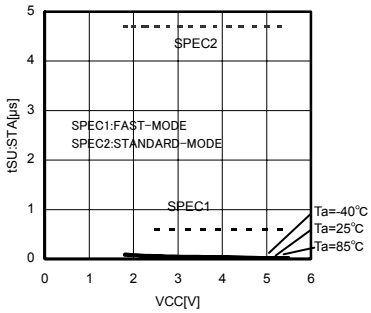


Fig.18 Start Condition Setup Time
tSU:STA

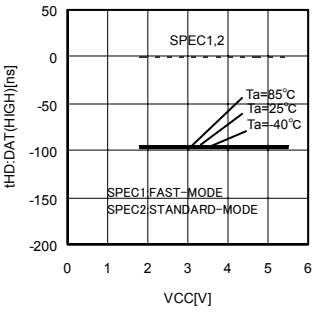


Fig.19 Input Data Hold Time
tHD:DAT(HIGH)

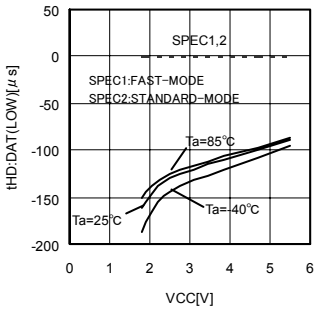


Fig.20 Input Data Hold Time
tHD:DAT(LOW)

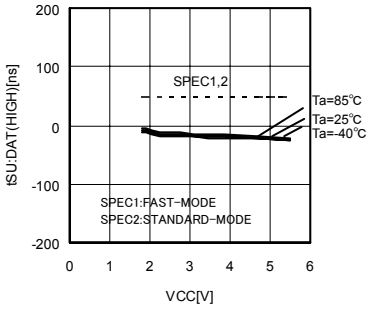


Fig.21 Input Data Setup Time
tSU:DAT(HIGH)

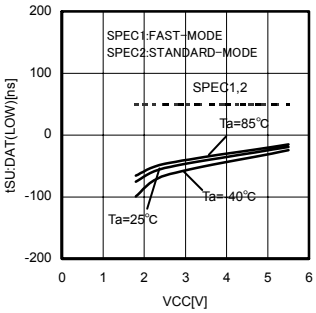


Fig.22 Input Data Setup Time
tSU:DAT(LOW)

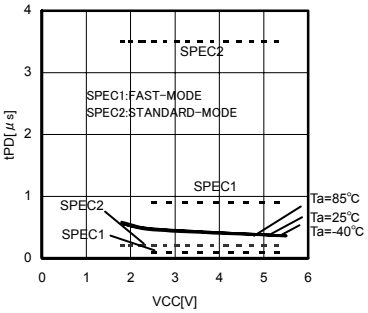


Fig.23 Output Data Delay Time
tPD

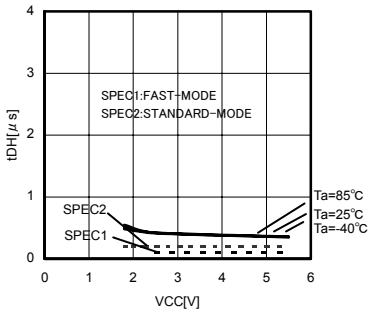


Fig.24 Output Data Hold Time
tDH

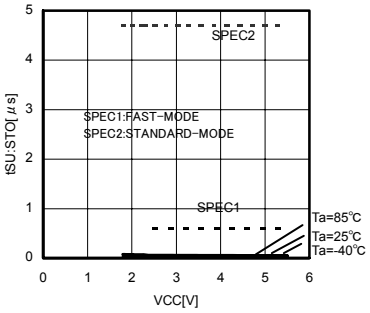


Fig.25 Stop Condition Setup Time
tSU:STO

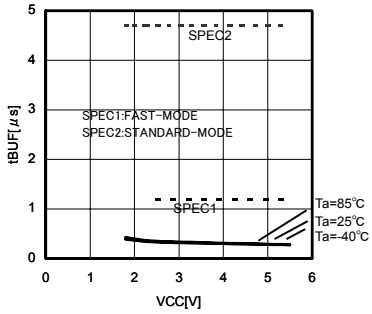


Fig.26 Bus Free Time
tBUF

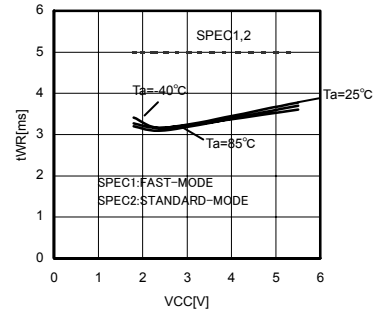


Fig.27 Write Cycle Time
tWR

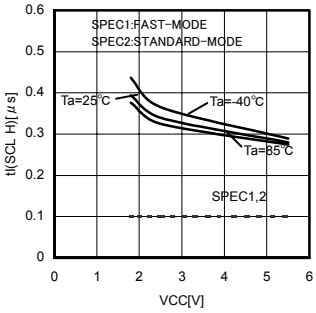


Fig.28 Noise Spike Width
tI(SCL H)

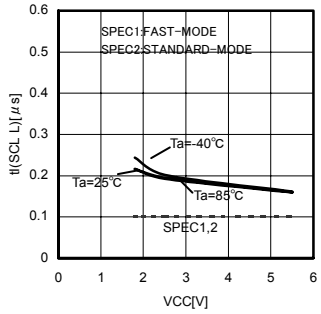


Fig.29 Noise Spike Width
tI(SCL L)

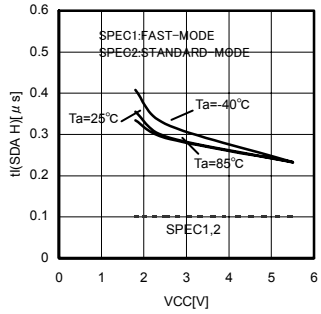


Fig.30 Noise Spike Width
tI(SDA H)

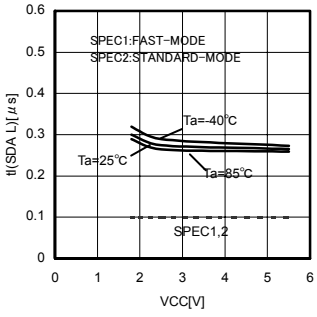


Fig.31 Noise Spike Width
tI(SDA L)

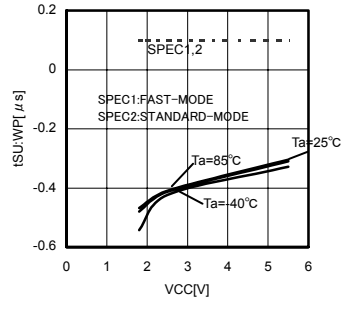


Fig.32 WP Setup Time
tSU:WP

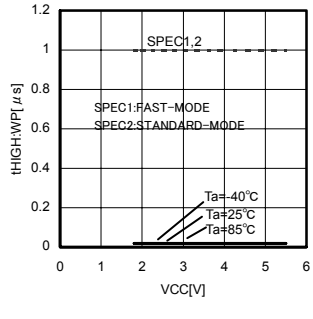


Fig.33 WP High Period
tHIGH:WP

●Data transfer on the I^2C-bus

○Data transfer on the I^2C-bus

The bus considered to be busy after the START condition, and be free again a certain time after the STOP condition.
Every byte put on the SDA line must be 8-bits long, and after each byte, the signal of a acknowledge is obligatory. The devices have the master and slave. The master is the device which initiates and ends a data transfer on the bus and generates the clock signals to permit that transfer.
The slave is the device which controlled with the unique address. EEPROM is slave. Also the device transmitting during transferring the data is called transmitter, and the device received is called receiver.

○START CONDITION (RECOGNITION OF START BIT)

- All commands are proceeded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH.
- The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. (See Fig.1-(b) START/STOP BIT TIMING)

○STOP CONDITION (RECOGNITION OF STOP BIT)

- All commands must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. (See Fig.1-(b) START/STOP BIT TIMING)

○ACKNOWLEDGE

- Acknowledge is a software convention used to indicate successful data transfers. The transmitter device will release the bus after transmitting eight bits. (When inputting the slave address in the write or read operation, transmitter is μ-COM. When outputting the data in the read operation, it is this device.)
- During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that the eight bits of data has been received. (When inputting the slave address in the write or read operation, receiver is this device. When outputting the data in the read operation, it is μ-COM.)
- The device will respond with an Acknowledge after recognition of a START condition and its slave address (8bit).
- In the WRITE mode, the device will respond with an Acknowledge, after the receipt of each subsequent 8-bit word (word address and write data).
- In the READ mode, the device will transmit eight bit of data, release the SDA line, and monitor the line for an Acknowledge.
- If an Acknowledge is detected, and no STOP condition is generated by the master, the device will continue to transmit the data. If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to the standby mode.

○DEVICE ADDRESSING

- Following a START condition, the master output the slave address to be accessed. The most significant four bits of the slave address are the “device type indentifier,” for the device this is fixed as “1010.” (In access to WP register, this code use "0110".)
- The next three bit (device address) identify the specified device on the bus. The device address is defined by the state of A0,A1 and A2 input pins. This IC works only when the device address inputted from SDA pin correspond to the state of A0,A1 and A2 input pins. Using this address scheme, up to eight devices may be connected to the bus. The last bit of the stream (R/$\overline{W}$…READ/$\overline{WRITE}$) determines the operation to be performed.

R/$\overline{W}$=0 WRITE (including word address input of Random Read)
R/$\overline{W}$=1 READ

Device Type	Device Address				
1010	A2	A1	A0	R/$\overline{W}$	Access to Memory
0110	A2	A1	A0	R/$\overline{W}$	Access to Write Protect Register

○WRITE PROTECT COMMAND

Write Protect Command is to cancel any write command which access to the address00～7Fh.
Write Protect Register can be written for once (Onetime Rom).
Once this command is excuted, the data is protected forever.

○WRITE PROTECT PIN(WP)

When WP pin set to Vcc (H level), write protect is set for 256 words (all address). When WP pin set to GND (L level), it is enable to write 256 words (all address).
If permanent protection is done by Write Protect command, lower half area (00～7Fh address) is inhibited writing regardless of WP pin state.
WP pin has a Pull-Down resistor. Please be left unconnected or connect to GND when WP feature is not in use.

●COMMAND

○WRITE CYCLE

With WRITE CYCLE operation, the given data is written in the EEPROM. BYTE WRITE CYCLE is usually used to write only one byte, but in case of writing continuous data more than one byte, it is possible with PAGE WRITE. The maximum bytes written at once is up to 16 bytes.

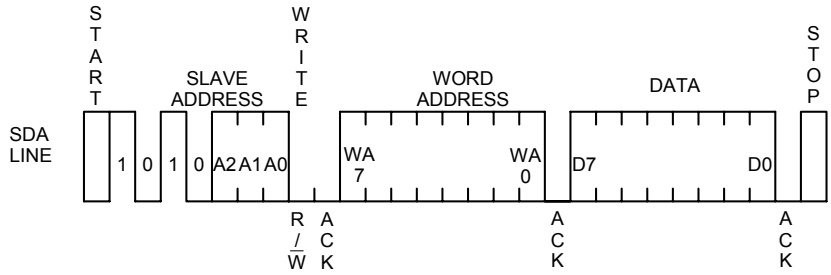


Fig.34 BYTE WRITE CYCLE TIMING

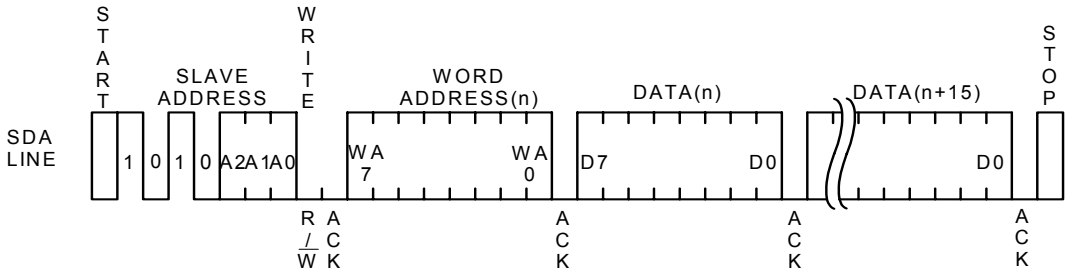


Fig.35 PAGE WRITE CYCLE TIMING

- By using this command, the data is programmed into the indicated word address.
- When the master generates a STOP condition, the device begins the internal write cycle to the nonvolatile memory array.
- This device is capable of sixteen byte Page Write operation.
- Once the programming is started, any commands isn't accept for tWR (5ms max.).
- If the master transmits more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previous transmitted data will be overwritten.
- When two or more byte data are inputted, the four low order address bits are internally incremented by one after the receipt of each word. The four higher order bits of the address(WA7～WA4) remain constant.

●COMMAND

○READ CYCLE

With READ CYCLE operation, the data is read from the EEPROM. READ CYCLE has RANDOM READ CYCLE and CURRENT READ CYCLE. RANDOM READ CYCLE is usually used to read the data in the indicated address.

Also CURRENT READ CYCLE is used to read the data in the address indicated internally and make a role of verifying the data immediately after WRITE OPERATION. The Sequential Read operation can be performed with both Current Read and Random Read. With SEQUENTIAL READ CYCLE, it is possible to read the next data continuously.

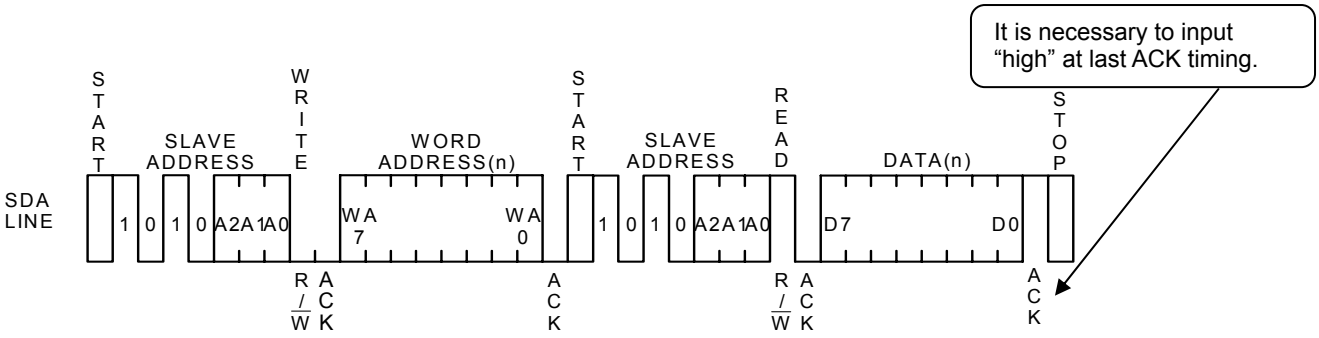


Fig.36 RANDOM READ CYCLE TIMING

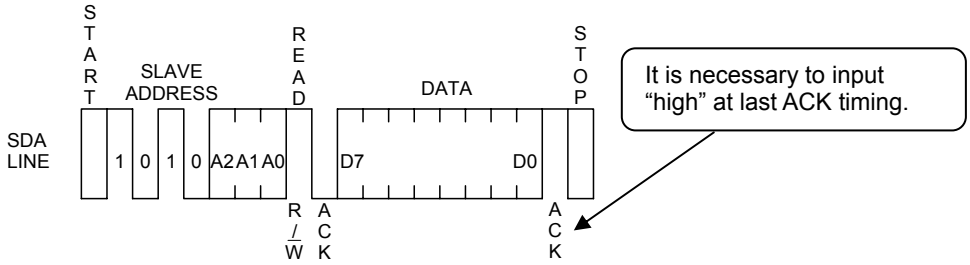


Fig.37 CURRENT READ CYCLE TIMING

- Random Read operation allows the master to access any memory location indicated by word address.
- In case that the previous operation is Random or Current Read (which includes Sequential Read respectively), the internal address counter is increased by one from the last accessed address (n). Thus Current Read outputs the data of the next word address (n+1).
- If an Acknowledge is detected, and no STOP condition is generated by the master (μ-COM), the device will continue to transmit the data. [It can transmit all data (2kbit 256word)]
- If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to the standby mode.
- If an Acknowledge is detected with "Low" level, not "High" level, command will become Sequential Read. So the device transmits the next data, Read is not terminated. In the case of terminating Read, input Acknowledge with "High" always, then input stop condition.

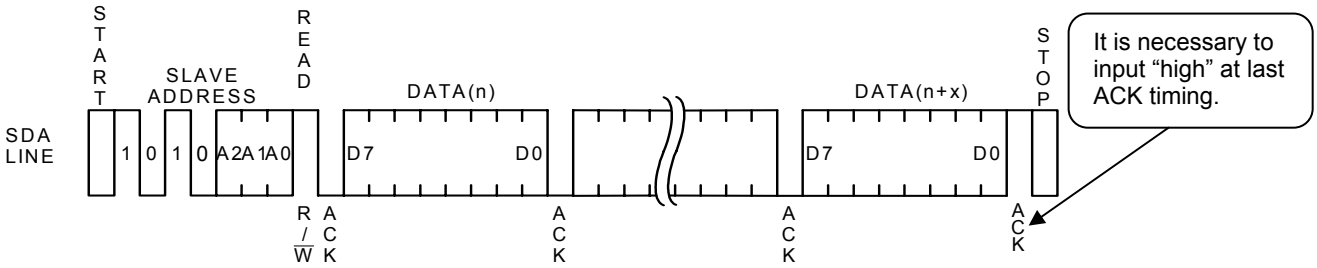


Fig.38 SEQUENTIAL READ CYCLE TIMING (With Current Read)

- If an Acknowledge is detected, and no STOP condition is generated by the master (μ-COM), the device will continue to transmit the data. [It can transmit all data (2kbit 256word)]
- If an Acknowledge is not detected, the device will terminate further data transmissions and await a STOP condition before returning to the standby mode.
- If an Acknowledge is detected with "Low" level, not "High" level, command will become Sequential Read. So the device transmits the next data, Read is not terminated. In the case of terminating Read, input Acknowledge with "High" always, then input stop condition.

●SOFTWARE RESET

Please execute software reset in case that the device is an unexpected state after power up and/or the command input need to be reset. There are some kinds of software reset. Here we show three types of example as follows.
During dummy clock, please release SDA bus (tied to Vcc by pull up resistor) .
During that time, the device may pull the SDA line LOW for acknowledge or outputting read data.
If the master controls the SDA line HIGH, it will conflict with the device output LOW then it makes a current overload. It may cause instantaneous power down and may damage the device.

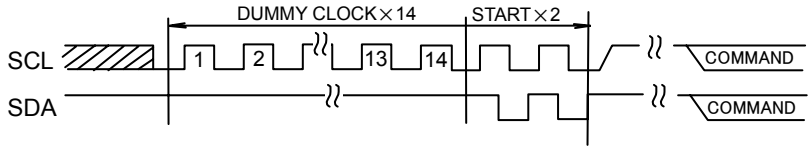


Fig.39-(a) DUMMY CLOCK×14 + START+START

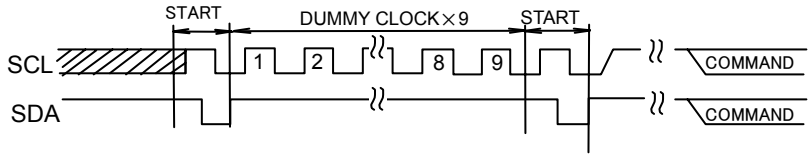


Fig.39-(b) START + DUMMY CLOCK×9 + START

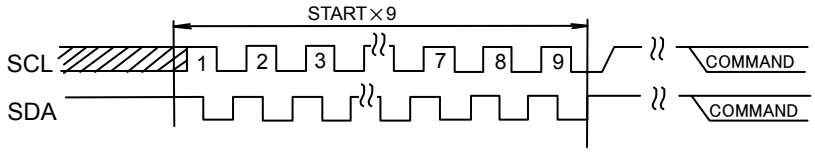


Fig.39-(c) START×9

＊ COMMAND starts with start condition.

●ACKNOWLEDGE POLLING

Since the device ignore all input commands during the internal write cycle, no ACK will be returned.
When the master send the next command after the write command, if the device returns the ACK, it means that the program is completed. If no ACK is returned, it means that the device is still busy.
By using Acknowledge polling, the waiting time is minimized less than tWR=5ms.
In case of operating Write or Current Read after Write, first, send the slave address (R/$\overline{W}$ is"HIGH" or "LOW" respectively).
After the device returns the ACK, continue word address input or data output respectively.

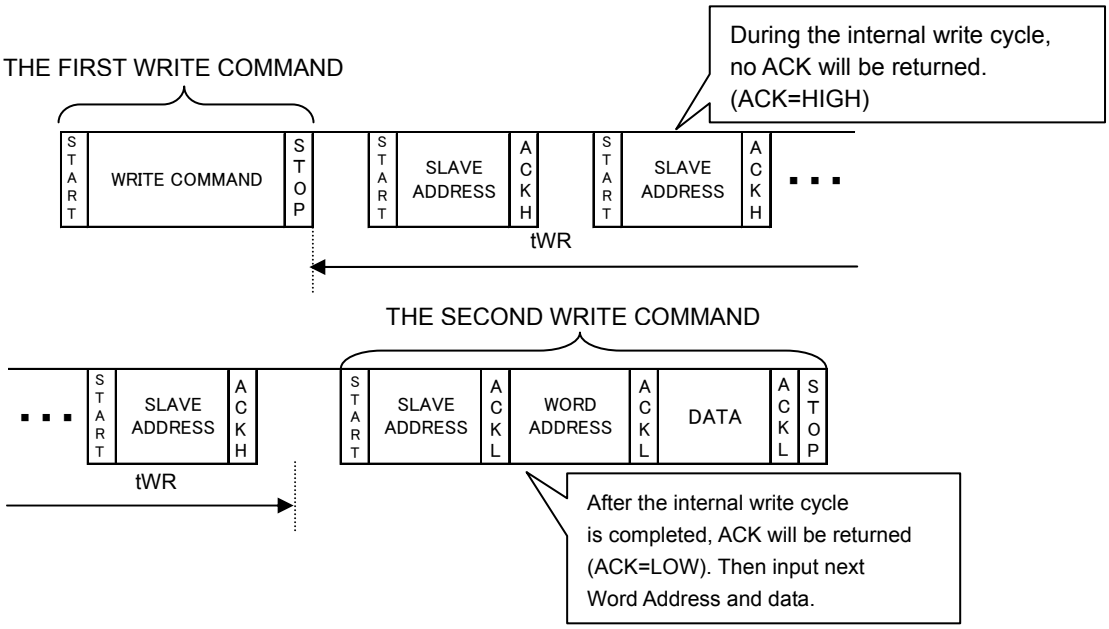


Fig.40 SUCCESSIVE WRITE OPERATION BY ACKNOWLEDGE POLLING

●WP EFFECTIVE TIMING

WP is fixed to "H" or "L" usually . But in case of controlling WP to cancel the write command, please pay attention to “WP effective timing” as follows.

During write command input , write command is canceled by controlling WP "H" within the WP cancellation effective period.

The period from the start condition to the rising edge of the clock which take in DO of the data (the first byte of the data for Page Write) is the cancellation invalid period. WP input is don't care during the period. Setup time for rising edge of the SCL which takes in DO must be more than 100ns.

The period from the rising edge of SCL which takes in DO to the end of internal write cycle (tWR) is the cancellation effective period. In case of setting WP to "H" during tWR, WRITE operation is stopped in the middle and the data of accessing address is not guaranteed, so that write correct data again please.

It is not necessary waiting tWR (5msMax.) after stopping command by WP, because the device is standby state.

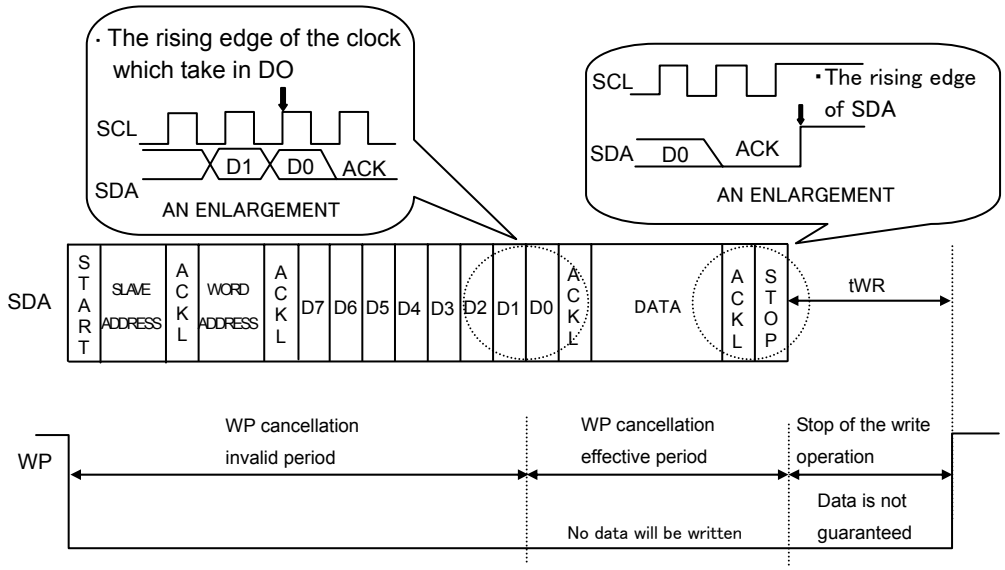


Fig.41 WP EFFECTIVE TIMING

●COMMAND CANCELLATION BY START AND STOP CONDITION

During a command input, it is canceled by the successive inputs of start condition and stop condition.(Fig.42)

But during ACK or data output, the device may output the SDA line LOW. In such cases, operation of start and stop condition is impossible, so that the reset can't work. Execute the software reset in the cases. (Fig.39)

Operating the command cancel by start and stop condition during the command of Random Read or Sequential Read or Current Read, internal address counter is not confirmed.

Therefore operation of Current Read after this is not valid. Operate a Random Read in this case.

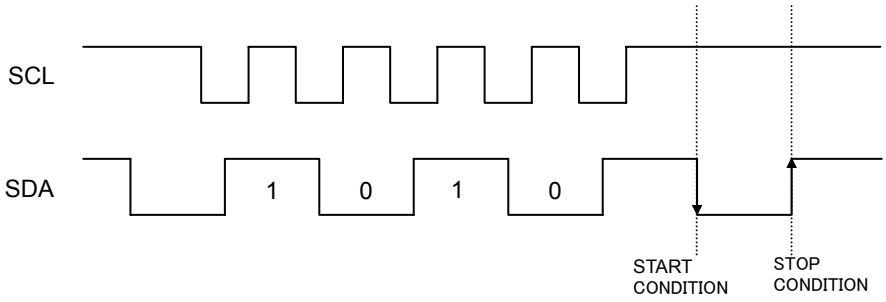


Fig.42 COMMAND CANCELLATION BY START AND STOP CONDITION DURING THE INPUT OF SLAVE ADDRESS

●I/O CIRCUIT

○PULL UP RESISTOR OF SDA PIN

The pull up resistor is needed because SDA is NMOS open drain. Decide the value of this resistor(R_{PU}) properly, by considering VIL, IL characteristics of a controller which control the device and VOL-IOL characteristics of the device. If large R_{PU} is chosen, clock frequency need to be slow. In case of small R_{PU} , the operating current increases.

○MAXIMUM OF R_{PU}

Maximum of R_{PU} is determined by following factors.

①SDA rise time determined by R_{PU} and the capacitance of bus line(CBUS) must be less than tR.
And the other timing must keep the conditions of AC specification.

②When SDA bus is HIGH, the voltage Ⓐ of SDA bus determined by a total input leakage(IL) of the all devices connected to the bus and R_{PU} must be enough higher than input HIGH level of a controller and the device, including noise margin 0.2V_{CC}.

$$V_{CC}-I_L R_{PU}-0.2\,V_{CC} \geqq V_{IH}$$

$$\therefore \quad R_{PU} \leqq \frac{0.8V_{CC}-V_{IH}}{I_L}$$

Examples: When V_{CC} =3V, IL=10μA, VIH=0.7 V_{CC}

According to ②

$$R_{PU} \leqq \frac{0.8\times3-0.7\times3}{10\times10^{-6}}$$

$$\leqq 300\ [k\Omega]$$

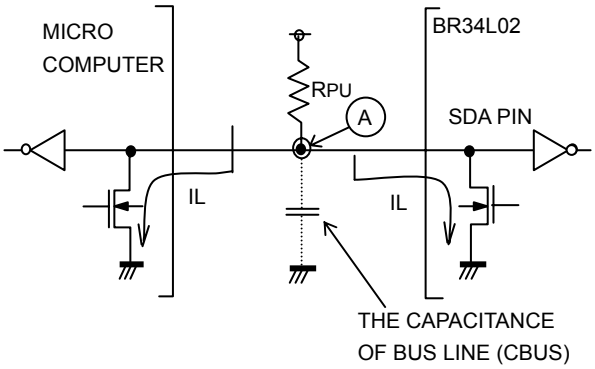


Fig.43 I/O CIRCUIT

○THE MINIMUM VALUE R_{PU}

The minimum value of R_{PU} is determined by following factors.

①Meet the condition that V_{OLMAX}=0.4V, I_{OLMAX}=3mA when the device output low on SDA line.

$$\frac{V_{CC}-V_{OL}}{R_{PU}} \leqq I_{OL}$$

$$\therefore \quad R_{PU} \geqq \frac{V_{CC}-V_{OL}}{I_{OL}}$$

②V_{OLMAX}(=0.4V) must be lower than the input LOW level of the controller and the EEPROM including recommended noise margin(0.1V_{CC}).

$$V_{OLMAX} \leqq V_{IL}-0.1\,V_{CC}$$

Examples: V_{CC}=3V, VOL=0.4V, IOL=3mA, the VIL of the controller and the EEPROM is VIL=0.3V_{CC},

According to ① $R_{PU} \geqq \frac{3-0.4}{3\times10^{-3}}$

$$\geqq 867\ [\Omega]$$

and V_{OL}=0.4 [V]

V_{IL}=0.3×3

=0.9 [V]

so that condition ② is met

○PULL UP RESISTOR OF SCL PIN

In the case that SCL is controlled by CMOS output, the pull up resistor of SCL is not needed.
But in the case that there is a timing at which SCL is Hi-Z, connect SCL to V_{CC} with pull up resistor.
Several～several dozen kΩ is recommended as a pull up resistor, which is considered with the driving ability of the output port of the controller.

●CONNECTIONS OF A0, A1, A2, WP PIN

○CONNECTIONS OF DEVICE ADDRESS PIN(A0, A1, A2)

The state of device address PIN are compared with the device address send by the master, then one of the devices which are connected to the identical bus is selected. Pull up or down these pins, or connect them to V_{CC} or GND. Pins which is not used as device address (N.C.PIN) may be either HIGH, LOW, and Hi-Z.

○CONNECTIONS OF WP PIN

The WP input allows or inhibits write operations. When WP is HIGH, only READ is available and WRITE to any address is inhibited. Both Read and Write are available when WP is LOW.
In the case that the device is used as a ROM, it is recommended that WP is pulled up or connected to V_{CC}. In the case that both READ and WRITE are operated, WP pin must be pulled down or connected to GND or controlled.

●THE NOTICE ABOUT THE CONNECTION OF CONTROLLER

○ABOUT Rs

The open drain interface is recommended for SDA port in I^2CBUS. But, in the case that Tri-state CMOS interface is applied to SDA, insert a series resistor Rs between SDA pin of the device and a pull up resistor R_{PU}. It limits the current from PMOS of controller to NMOS of EEPROM.

Rs also protects SDA pin from surges. Therefore, Rs is able to be used though SDA port is open drain.

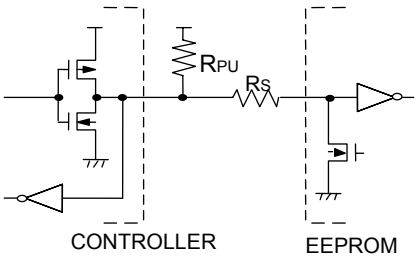


Fig.44 I/O CIRCUIT

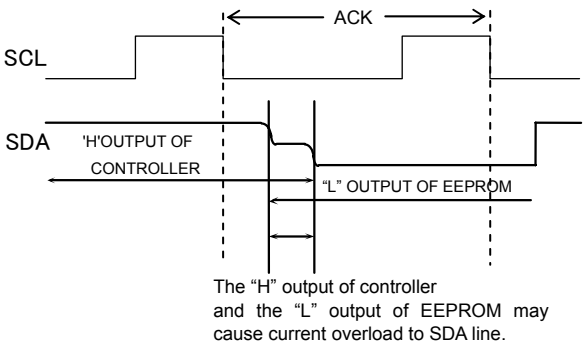


Fig.45 INPUT/OUTPUT COLLISION TIMING

○THE MAXIMUM VALUE OF Rs

The maximum value of Rs is determined by following factors.

①SDA rise time determined by R_{PU} and the capacitance of bus line(CBUS) of SDA must be less than tR. And the other timing must also keep the conditions of the AC timing.

②When the device outputs LOW on SDA line, the voltage of the bus Ⓐ determined by R_{PU} and Rs must be lower than the inputs LOW level of the controller, including recommended noise margin(0.1V_{CC}).

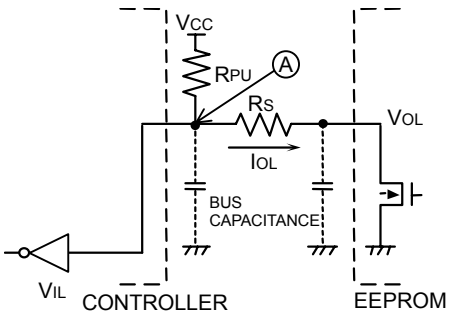


Fig.46 I/O CIRCUIT

$$\frac{(V_{CC}-V_{OL})\times R_S}{R_{PU}+R_S} + V_{OL}+0.1V_{CC} \leqq V_{IL}$$

$$\therefore\ R_S \leqq \frac{V_{IL}-V_{OL}-0.1V_{CC}}{1.1V_{CC}-V_{IL}} \times R_{PU}$$

Examples : When V_{CC}=3V V_{IL}=0.3V_{CC} V_{OL}=0.4V R_{PU}=20kΩ

According to ② $R_S \leqq \frac{0.3\times3-0.4-0.1\times3}{1.1\times3-0.3\times3} \times 20\times10^3$

$\leqq$ 1.67 [kΩ]

○THE MINIMUM VALUE OF Rs

The minimum value of Rs is determined by the current overload due to the conflict on the bus.

The current overload may cause noises on the power line and instantaneous power down.

The following conditions must be met, where I is the maximum permissible current.

The maximum permissible current depends on Vcc line impedance and so on. It need to be less than 10mA for EEPROM.

$$\frac{Vcc}{R_S} \leqq I$$

$$\therefore\ R_S \geqq \frac{Vcc}{I}$$

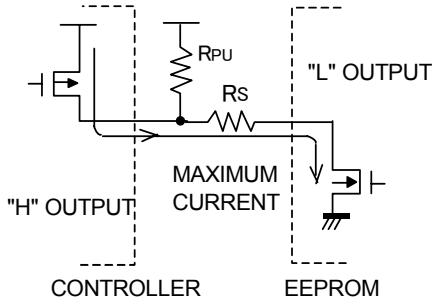


Fig.47 I/O CIRCUIT

Examples: When V_{CC}=3V, I=10mA

$$R_S \geqq \frac{3}{10\times10^{-3}}$$

$\geqq$ 300 [Ω]

●I^2C BUS INPUT / OUTPUT CIRCUIT

○INPUT(A0,A2,SCL)

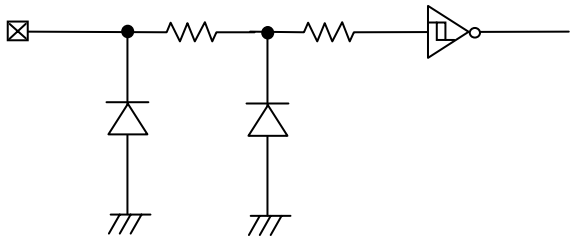


Fig.48 INPUT PIN CIRCUIT

○INPUT / OUTPUT (SDA)

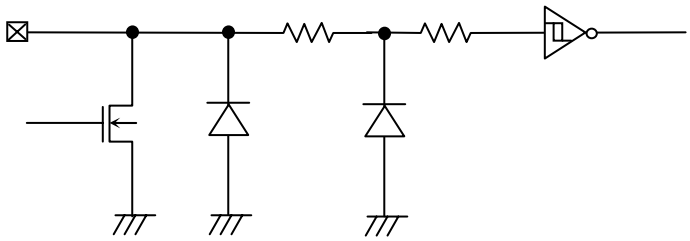


Fig.49 INPUT / OUTPUT PIN CIRCUIT

○INPUT (A1)

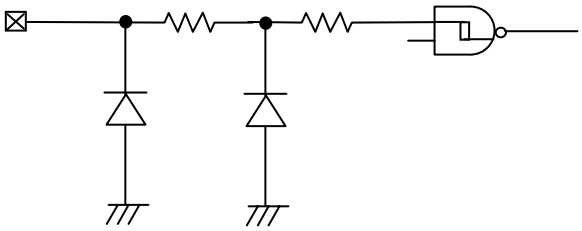


Fig.50 INPUT PIN CIRCUIT

○INPUT (WP)

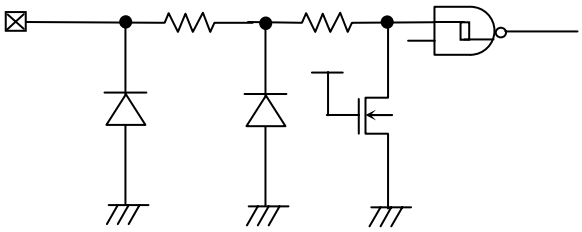


Fig.51 INPUT PIN CIRCUIT

●NOTES FOR POWER SUPPLY

Vcc rises through the low voltage region in which internal circuit of IC and the controller are unstable, so that device may not work properly due to an incomplete reset of internal circuit. To prevent this, the device has the feature of P.O.R. and LVCC. In the case of power up, keep the following conditions to ensure functions of P.O.R. and LVCC.

1. It is necessary to be "SDA='H'" and "SCL='L' or 'H'".
2. Follow the recommended conditions of tR, tOFF, Vbot for the function of P.O.R. during power up.

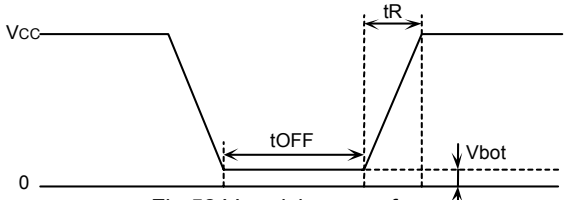


Fig.52 Vcc rising wavefrom

Recommended conditions of tR, tOFF, Vbot

tR	tOFF	Vbot
Below 10ms	Above 10ms	Below 0.3V
Below 100ms	Above 10ms	Below 0.2V

3. Prevent SDA and SCL from being "Hi-Z".

In case that condition 1. and/or 2. cannot be met, take following actions.

A）Unable to keep condition 1.(SDA is "LOW" during power up.)

→Control SDA ,SCL to be "HIGH" as figure below.

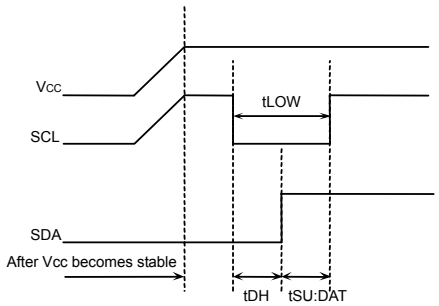


Fig.53 SCL="H" and SDA="L"

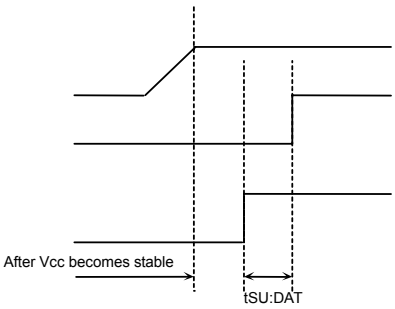


Fig.54 SCL="L" and SDA="L"

B）Unable to keep condition 2.

→After power becomes stable, execute software reset. (See page 10/16)

C）Unable to keep both conditions 1 and 2.

→Follow the instruction A first, then the instruction B.

●LVCC CIRCUIT

LVCC circuit inhibit write operation at low voltage, and prevent an inadvertent write. Below the LVCC voltage（Typ.=1.2V）, write operation is inhibited.

●NOTES FOR NOISE ON Vcc

○ABOUT BYPASS CAPACITOR

Noise and surges on power line may cause the abnormal function. It is recommended that the bypass capacitors (0.1μF) are attached on the Vcc and GND line beside the device.

The attachment of bypass capacitors on the board near by connector is also recommended.

●CAUTIONS ON USE

(1)Absolute maximum ratings

If the absolute maximum ratings such as impressed voltage and action temperature range and so forth are exceeded, LSI may be destructed. Do not impress voltage and temperature exceeding the absolute maximum ratings. In the case of fear exceeding the absolute maximum ratings, take physical safety countermeasures such as fuses, and see to it that conditions exceeding the absolute maximum ratings should not be impressed to LSI.

(2) GND electric potential

Set the voltage of GND terminal lowest at any action condition. Make sure that each terminal voltage is lower than that of GND terminal.

(3) Thermal design

In consideration of permissible loss in actual use condition, carry out heat design with sufficient margin.

(4) Terminal to terminal shortcircuit and wrong packaging

When to package LSI onto a board, pay sufficient attention to LSI direction and displacement. Wrong packaging may destruct LSI. And in the case of shortcircuit between LSI terminals and terminals and power source, terminal and GND owing to foreign matter, LSI may be destructed.

(5) Use in a strong electromagnetic field may cause malfunction, therefore, evaluated design sufficiently.

●SELECTION OF ORDER TYPE

BR	34	L	02	FV	—	W	E2
ROHM type	BUS type 34:I^2C	Product type L:1.8Vversion *	Capacity 02=2K	Package FV:SSOP-B8 FVT:TSSOP-B8		Double Cell	Package specifications E2:reel shape emboss taping

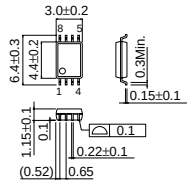
*1.7V version only for BR34L02-W

●PACKAGE SPECIFICATIONS

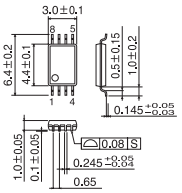
SSOP-B8/TSSOP-B8

<Dimension>

・SSOP-B8



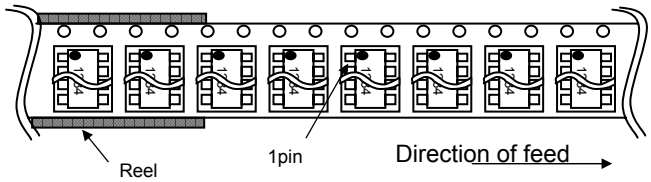
・TSSOP-B8



(Unit:mm)

<Tape and Reel information> SSOP-B8/TSSOP-B8

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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